CLAIMS

We claim:

1. An apparatus comprising:

a data aligner to receive a data stream from a data transmission link and to separate the received data stream into a segment of predefined number of bytes to identify data bytes for alignment, wherein the data has a granularity of less than a width of an internal data path, the data aligner to align a fragment of data with a current segment or delay the fragment to combine with a next segment for alignment into interim storage for subsequent output onto the internal data path; and

a buffer to receive aligned data from the data aligner for interim storage and to output data onto the internal data path.

2. The apparatus of claim 1 further including a control decode logic to separate commands from data at an input to the data aligner and to process commands to align the data.

3. The apparatus of claim 2, wherein the data aligner includes a multiplexing circuit to multiplex certain minimum contiguous bytes of data for the alignment into the interim storage, the multiplexing circuit selecting from current and delayed fragments to obtain alignment of data.

4. The apparatus of claim 3, wherein the data aligner includes a multiplexer control logic to control the multiplexing circuit.

5. The apparatus of claim 4, wherein the multiplexer control logic includes at least one state machine to generate a select signal to the multiplexing circuit to control fragment byte selection for alignment.

6. The apparatus of claim 5, wherein the at least one state machine enables bytes output from the multiplexing circuit when the output bytes are data bytes.

7. The apparatus of claim 6, wherein the data aligner to receive data is based on the SPI-4 protocol.

8. An apparatus comprising:

a data aligner to receive a data stream from a data transmission link and to separate the received data stream into a segment of eight bytes to identify data bytes for alignment, wherein the data has a granularity set to two bytes (double-byte) and in which

the aligner to align a double-byte fragment of data with a current segment or delay the fragment to combine with a next segment for alignment into interim storage for subsequent output onto an internal data path; and

a buffer to receive aligned data from the data aligner for interim storage and to output data onto the internal data path.

9. The apparatus of claim 8 further including a control decode logic to separate commands from data at an input to the data aligner and to process commands to align the data.

10. The apparatus of claim 9, wherein the data aligner includes a multiplexing circuit to multiplex two pairs of double-byte words, but in which alignment of the pairs of double-byte words places even numbered double-byte data word at a beginning of the eight-byte segment to alignment the data.

11. The apparatus of claim 10, wherein the data aligner includes a multiplexer control logic to control the multiplexing circuit, wherein the multiplexer control logic includes at least one state machine to generate a select signal to the multiplexing circuit to control double-byte fragment selection for output from the multiplexing circuit to obtain alignment of data.

12. The apparatus of claim 11, wherein the at least one state machine enables certain double-byte output from the multiplexing circuit when the certain double-byte output is a double-byte data word.

13. The apparatus of claim 12, wherein the data aligner to receive data is based on the SPI-4 protocol.

14. An integrated circuit comprising:

an interface unit to receive incoming data stream from a data transmission link for use by the integrated circuit;

a control decode logic operably coupled to the interface unit to receive and separate commands from the incoming data stream for use to align data;

a data aligner to receive data from the interface unit and to segment the received data into a segment of eight bytes to identify data bytes for alignment, wherein the data has a granularity set to two bytes (double-byte) and in which the data aligner to align a double-byte fragment of data with a current segment or delay the fragment to combine

with a next segment for alignment into interim storage for subsequent output onto an internal data path; and

a buffer to receive aligned data from the data aligner for interim storage and to output data onto the internal data path.

15. The integrated circuit of claim 14, wherein the data aligner includes a multiplexing circuit to multiplex two pairs of double-byte words, but in which alignment of the pairs of double-byte words places even numbered double-byte data word at a beginning of the eight-byte segment to obtain alignment of data.

16. The integrated circuit of claim 15, wherein the data aligner includes a multiplexer control logic to control the multiplexing circuit, wherein the multiplexer control logic includes at least one state machine to generate a select signal to the multiplexing circuit to control double-byte fragment selection for output from the multiplexing circuit to obtain alignment of data.

17. The integrated circuit of claim 16, wherein the at least one state machine enables certain double-byte output from the multiplexing circuit when the certain double-byte output is a double-byte data word.

18. The integrated circuit of claim 17, wherein the data aligner to receive data is based on the SPI-4 protocol.

19. A method comprising:

segmenting a data stream received from a data transmission link by separating the received data stream into a segment of eight bytes to identify data bytes for alignment, wherein the data has a granularity set to two bytes (double-byte);

aligning the eight bytes so that a double-byte fragment is aligned with the current segment or delayed to combine with a next segment for alignment into interim storage for subsequent output onto an internal data path;

multiplexing two pairs of double-byte word groups for output, but in which alignment of the pairs of double-byte words places even numbered double-byte data word at a beginning of the eight-byte segment to obtain alignment of data; and

buffering aligned data into interim storage to output data onto the internal data path.

20. The method of claim 19, wherein the segmenting the data stream segments data based on SPI-4 protocol.